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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,492	04/12/2006	Shinji Maekawa	740756-2947	3788

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EXAMINER	
ISAAC, STANETTA D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,492	MAEKAWA ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16,17,19,20 and 26* is/are allowed.

6)☒ Claim(s) *1-9,11-15,18,21-25 and 28-35* is/are rejected.

7)☒ Claim(s) *10 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :4/12/06, 5/26/06, 7/26/06, and 10/30/06.

DETAILED ACTION

This Office Action is in response to the application filed on 4/12/06. Currently, claims 1-35 are pending.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statements (IDS) were submitted on 4/12/06, 5/26/06, 7/26/06, and 10/30/06. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 8 and 21-24 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim does not refer back in the alternative only. See MPEP § 608.01(n). Accordingly, the claims 8 and 21-24 has not been further treated on the merits.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. In lines 4-8, It s indefinite, whether the semiconductor film is formed over the source and drain regions, respectively or if the gate electrode is formed above the semiconductor film or under.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 3, 5-9, 11-15, 21, 23-26, and 29-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al., US Patent Application Publication US 2003/0083203.

Hashimoto discloses the semiconductor method as claimed. See figures 1-13, and corresponding text, where Hashimoto teaches, pertaining to claim 1, a method for forming a wiring comprising the steps of: performing a liquid-repellent treatment on a surface ([0087] and [0097-0098]); performing selectively a lyophilic treatment on a region of the surface ([0100]);

and forming a wiring on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto teaches, pertaining to claim 2, a method for forming a wiring comprising the steps of: forming a liquid-repellent region on a surface ([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region ([0100]); and forming the wiring on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto teaches, pertaining to claim 3, a method for forming a wiring comprising the steps of: forming a liquid-repellent region on a surface by a plasma treatment([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region ([0100]); and forming the wiring on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto teaches, pertaining to claim 6, wherein the lyophilic region is selectively formed by irradiating the liquid-repellent region with laser light ([0100]).

Hashimoto teaches, pertaining to claim 7, wherein a region that is less liquid-repellent than the liquid-repellent region is formed as the lyophilic region ([0100]).

Hashimoto teaches, pertaining to claim 8, wherein the composition is dropped by an ink-jetting method ([0106]).

Hashimoto teaches, pertaining to claim 9, a method for forming a wiring comprising the steps of: forming a liquid-repellent region by forming a film containing fluorine on a surface ([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region([0100]); and forming the wiring on the lyophilic region by dropping a composition including a conductive material([0102]).

Hashimoto teaches, pertaining to claim 11, wherein the lyophilic region is selectively formed by irradiating the liquid-repellent region with laser light ([0100]).

Hashimoto teaches, pertaining to claim 12, wherein a region that is less liquid-repellent than the liquid-repellent region is formed as the lyophilic region ([0100]).

Hashimoto teaches, pertaining to claim 13, wherein the composition is dropped by an ink-jetting method ([0106]).

Hashimoto teaches pertaining to claim 14, a method for manufacturing a thin film transistor comprising the steps of: performing a liquid-repellent treatment on a surface ([0087] and [0097-0098]); performing selectively a lyophilic treatment on a region of the surface ([0100]); and forming a conductive film on the lyophilic treatment by dropping a composition including a conductive material ([0102]).

Hashimoto teaches, pertaining to claim 15, a method for manufacturing a thin film transistor comprising the steps of: forming a liquid-repellent region on a surface ([0087] and [0097-0098]); forming selectively a lyophilic region in the liquid-repellent region ([0100]), and forming the conductive film on the lyophilic region by dropping a composition including a conductive material ([0102]).

Hashimoto teaches, pertaining to claim 21, wherein the liquid-repellent region is formed by forming a CF.sub.2 bond on the surface by the plasma treatment ([0087] and [0097-0098]).

Hashimoto teaches, pertaining to claim 23, wherein the liquid-repellent region is irradiated with laser light to selectively form the lyophilic region ([0100]).

Hashimoto teaches, pertaining to claim 24, wherein the composition is dropped by an ink-jetting method ([0102]).

Hashimoto teaches, pertaining to claim 25, a method for manufacturing a thin film transistor, comprising the steps of: forming a film containing fluorine ([0087] and [0097-0098]); forming selectively a lyophilic region in the film containing fluorine ([0100]); forming a gate electrode on the lyophilic region by dropping a composition including a conductive material ([0102]); and performing a heat treatment for baking the gate electrode, and removing the film containing fluorine by the heat treatment ([0100]).

Hashimoto teaches, pertaining to claim 29, wherein the liquid-repellent region is irradiated with laser light to selectively form the lyophilic region ([0100]).

Hashimoto teaches, pertaining to claim 30, wherein the composition is dropped by an ink-jetting method ([0102]).

Hashimoto teaches, pertaining to claim 31, a droplet discharging method, comprising the steps of: forming a lyophilic region by irradiating selectively on an object to be treated in which a liquid-repellent region is formed with light by a light irradiation unit([0087] and [0097-0098]; ([0100])); and discharging a droplet onto the lyophilic region by a droplet discharging unit, in a treatment chamber including the droplet discharging unit and the light irradiation unit ([0102]).

Hashimoto teaches, pertaining to claim 32, a droplet discharging method, using a treatment apparatus in which a first treatment chamber having a plasma unit and a dielectric, and a second treatment chamber having a droplet discharging unit and a light irradiation unit, comprising the steps of: forming a liquid-repellent region in an object to be treated by the plasma unit and the dielectric in the first treatment chamber ([0087] and [0097-0098]); transporting the object to be treated into the second treatment chamber without being exposed to the atmosphere; forming selectively a lyophilic region in the object to be treated in which a liquid-repellent

region is formed by the light irradiation unit in the second treatment chamber ([0100]); and discharging a droplet onto the lyophilic region by the droplet discharging unit ([0102]).

Hashimoto teaches, pertaining to claim 33, wherein the droplet discharging unit and the light irradiation unit are integrally formed ([0115]).

Hashimoto teaches, pertaining to claim 34, wherein the light irradiation unit includes laser light ([0115}).

Pertaining to claim 35, wherein the composition is dropped by an ink-jetting method ([0102]).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 18, 22, and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi US Patent Application Publication US 2005/0040759 (as best understood by the Examiner).

Kobayashi discloses the semiconductor method as claimed. See figures 1-23C, and corresponding text, where Kobayashi teaches, pertaining to claim 18, a method for manufacturing a thin film transistor, comprising the steps of: forming a source electrode **141a** and a drain electrode **141b** (figure 4; [0067]); forming a semiconductor film **141** over the source electrode and the drain electrode (figure 4; [0065]); forming a liquid-repellent region by performing a plasma treatment on a surface for forming a gate electrode **111** in an upper portion of the semiconductor film (figure 7; [0091]); forming selectively a lyophilic region in the liquid-

repellent region [0096]; and forming the gate electrode **111** in the lyophilic region of the surface of the gate electrode by dropping a composition including a conductive material [0118]).

Kobayashi teaches, pertaining to claim 22, comprising the steps of: forming an interlayer insulating film **112** over the thin film transistor (figure 6; [0084]); forming an opening portion **112d** in the interlayer insulating film (figure 6; [0087]); forming a liquid-repellent region in a surface of the opening portion and the interlayer insulating film by performing a plasma treatment on the interlayer insulating film in which the opening portion is formed ([0089]); forming selectively a lyophilic region in the opening portion of the liquid-repellent region [0096]); and forming a wiring **110d** to be connected to a source electrode or a drain electrode of the thin film transistor through the opening portion by dropping a composition including a conductive material (figure 11; [0128-0134).

Kobayashi teaches, pertaining to claim 28, comprising the steps of: forming an interlayer insulating film **112** over the thin film transistor (figure 6; [0084]); forming an opening portion **112d** in the interlayer insulating film (figure 6; [0087]); forming a liquid-repellent region in a surface of the opening portion and the interlayer insulating film by performing a plasma treatment on the interlayer insulating film in which the opening portion is formed ([0089]); forming selectively a lyophilic region in the opening portion of the liquid-repellent region [0096]); and forming a wiring **110d** to be connected to a source electrode or a drain electrode of the thin film transistor through the opening portion by dropping a composition including a conductive material (figure 11; [0128-0134).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al., US Patent Application Publication US 2003/0083203.

4. Hashimoto discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1, 2, 3, 5-9, 11-15, 18, 21, 23, 24, 26, and 29-32. In addition, Hashimoto shows, pertaining to claim 5, wherein the plasma treatment is performed under an atmospheric pressure or a pressure in a neighborhood of an atmospheric pressure by using air, oxygen or nitrogen as a treatment gas ([0097]).

5. However, Hashimoto fails to show, pertaining to claim 4, wherein the plasma treatment is performed at a pressure of 100 Torr to 1000 Torr.

6. Hashimoto teaches performing a plasma treatment to create a liquid repellent.

7. It would have been obvious to one of ordinary skill in the art to incorporate, wherein the plasma treatment is performed at a pressure of 100 Torr to 1000 Torr, in the method of Hashimoto, pertaining to claim 4, according to the teachings of Hashimoto, with the motivation that pressure are parameters of optimization, where one of ordinary skill in the art would be capable of producing the above pressure during routine experimentation.

Allowable Subject Matter

8. Claims 10 and 27are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9.

10. Claims 16, 17, 19, 20 and 26 are allowed over the prior art of record (subjected to further consideration and/or search).

11. The following is an examiner's statement of reasons for allowance:

12. The closest prior art of record, Hashimoto et al., US Patent Application Publication US 2003/0083203 and Kobayashi US Patent Application Publication US 2005/0040759, fails to show, the following steps of:

13. Pertaining to independent claim 16, "forming a second liquid-repellent region by a plasma treatment on a surface for forming a source electrode and drain electrode; forming selectively a second lyophilic region in the second liquid repellent region;"

14. Pertaining to independent claim 17, "forming a second liquid-repellent region by plasma treatment on the semiconductor film having one conductivity and gate insulating film; forming selectively a second lyophilic region in the second liquid repellent region;"

15. Pertaining to independent claim 19, "forming a second liquid-repellent region by performing a plasma treatment on the gate insulating film; forming selectively a second lyophilic in the second repellent region;"

16. Pertaining to independent claim 20, "forming a second liquid-repellent region by plasma treatment on the semiconductor film; forming selectively a second lyophilic region in the second repellent region;"

17. Pertaining to independent claim 26,"forming a second film containing fluorine over the semiconductor film having one conductivity and the gate insulating film; forming selectively a second lyophilic region in the second film containing fluorine;"

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
January 6, 2008